ABSTRACT

The delay circuit composed of plural flip-flops converts an input data into plural data 110-0 ~ 110-n having delays of 1 ~ n clocks, which are inputted to the selector of the selector circuit. The counter counts the pixel number per one line of the input data, and supplies a discrete value signal indicating the counted pixel number to the judgment circuit of the selector. The judgment circuit calculates a difference between the standard pixel number and the pixel number that the discrete value signal indicates, and calculates a new delay to the delay circuit on the basis of this calculated difference. The selector outputs an output data based on the new delay calculated. With a simplified circuit configuration as above, the pixel number for each line will be regulated into the standard pixel number.